RA-SR: A 16–32-Channel Low-Power FPGA Multi-Protocol ESC Controller for Space Robotics

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RA-SR on Drones

Why RA-SR? Vision for Next-Gen Space Robotics

Scaling demands:

- Urban eVTOL “air taxis” with **36** ducted fans
- Martian rotorcraft requiring **16+** rotors for thin-CO_2 lift
- In-orbit servicers with **24–32** micro-thrusters for precision docking

Limitations of today’s ESCs:

- MCU-based controllers capped at **4–8 channels** (jitter ≥ 1 µs)
- High per-channel power (≈ 2.5 W) and CPU overhead
- No unified multi-protocol support (**PWM, PPM, DShot**) beyond 8 channels

Our goals:

- Deterministic timing (< 50 ns jitter) entirely in FPGA fabric
- Scalability to **16–32 channels** with zero CPU load
- Energy efficiency (≤ 1 W/channel at hover) for long-duration missions

Limitations of Today’s ESC Controllers

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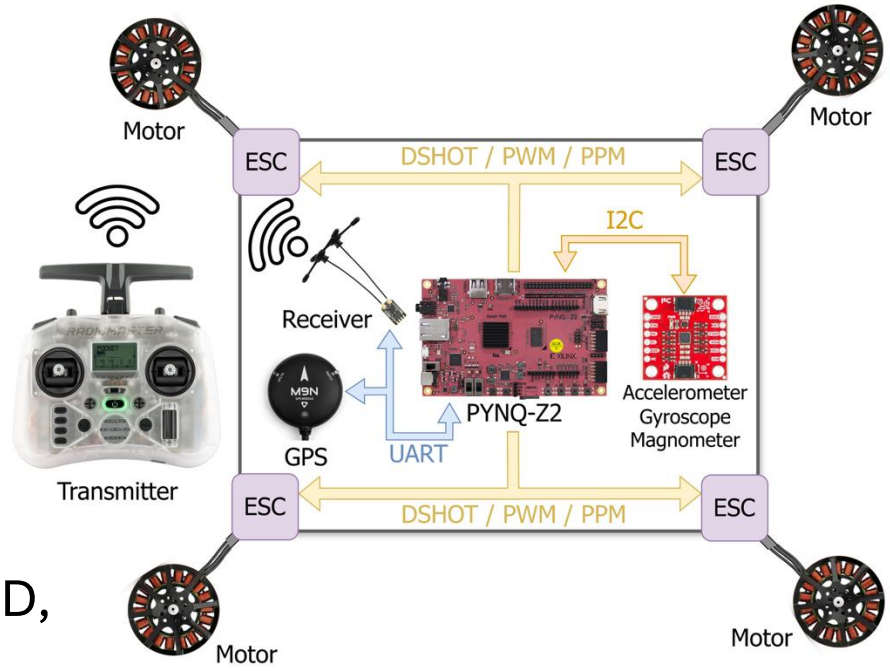
- **Channel count capped**
  - MCU-based boards: only 4–8 channels (STM32 series)
  - Pixhawk 4: max 8 channels
- **High & unpredictable latency**
  - Jitter ≥ 1 µs on MCU-based controllers (STM32 series)
  - Hybrid MCU+FPGA still sees ~ 0.5 µs latency
- **Elevated power draw**
  - ≈ 2.3–2.5 W per channel on commercial autopilots
- **CPU overhead**
  - Interrupt-driven PWM/PPM on MCUs consumes CPU cycles, reducing compute headroom
- **Single-protocol or partial support**
  - Most FPGA implementations handle only one protocol (e.g., PWM or DShot)

RA-SR System Architecture

Key Components & Data Flow:

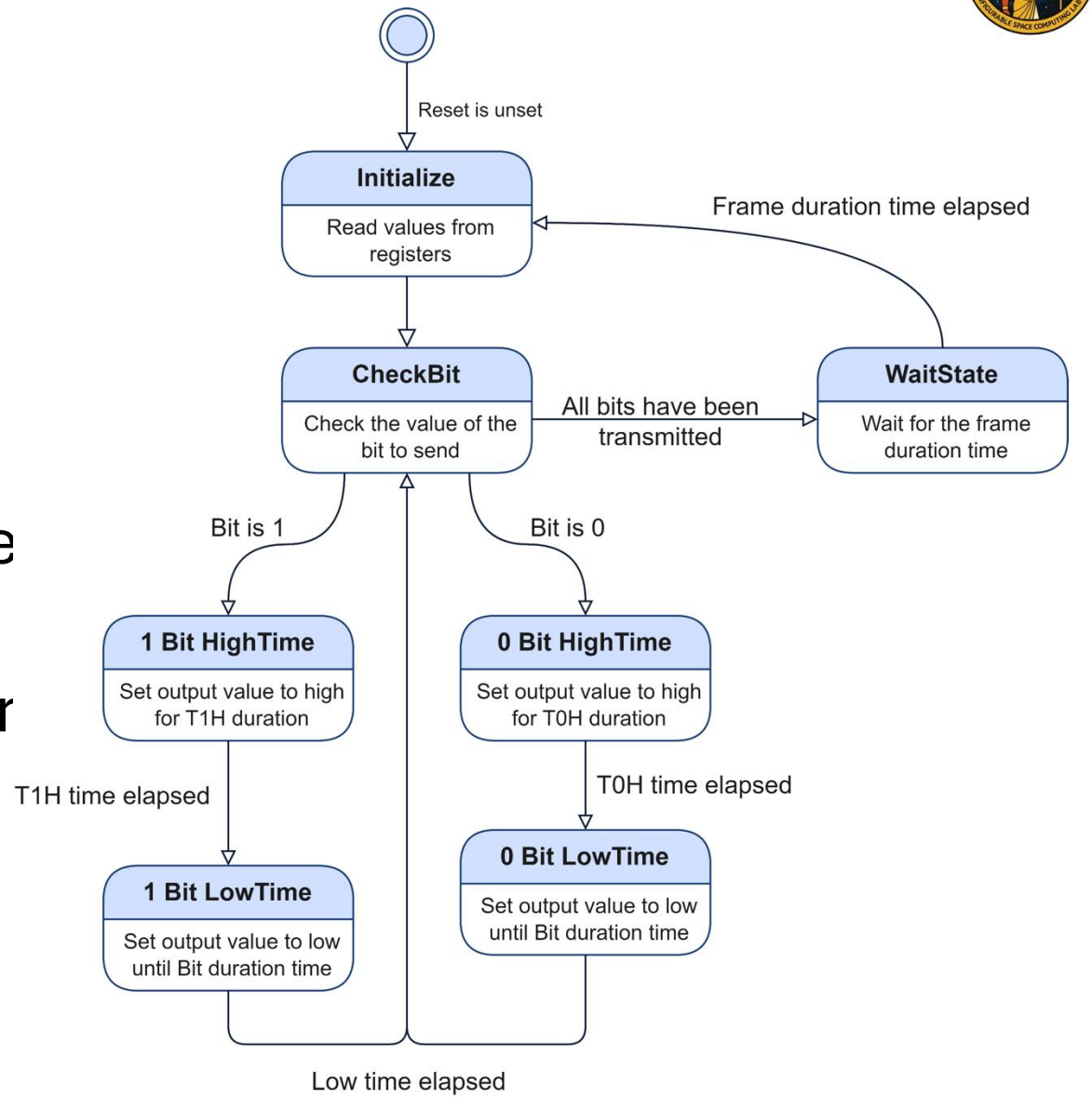
- **SoC Platform:**
  - Xilinx Zynq PYNQ-Z2 (FPGA fabric + dual ARM Cortex-A9 cores)
- **Programmable Logic (PL):**
  - Dedicated FSM IP cores for **PWM**, **PPM**, and **D-Shot**
  - Hardware protocol selector (crossbar) for per-channel dynamic switching
  - Offloads all timing-critical tasks → **< 50 ns jitter**, zero CPU overhead
- **Processing System (PS):**
  - **MicroBlaze soft-core** (early prototypes, up to 16 channels)
  - **ARM Cortex-A9** for full 32 channel management, closed-loop PID, telemetry
  - AXI Timer IP for latency profiling
- **Peripherals & Interfaces:**
  - **ESC Array:** 16–32 brushless ESCs
  - **Sensors:** IMU (I^2C), GPS (UART)
  - **Telemetry:** AXI-Lite bus for voltage/current ADC, real-time logging
  - **Radio RX:** ELRS/UART or equivalent



Multi-Protocol FSMs for ESC Control

Dedicated FSM IP Cores:

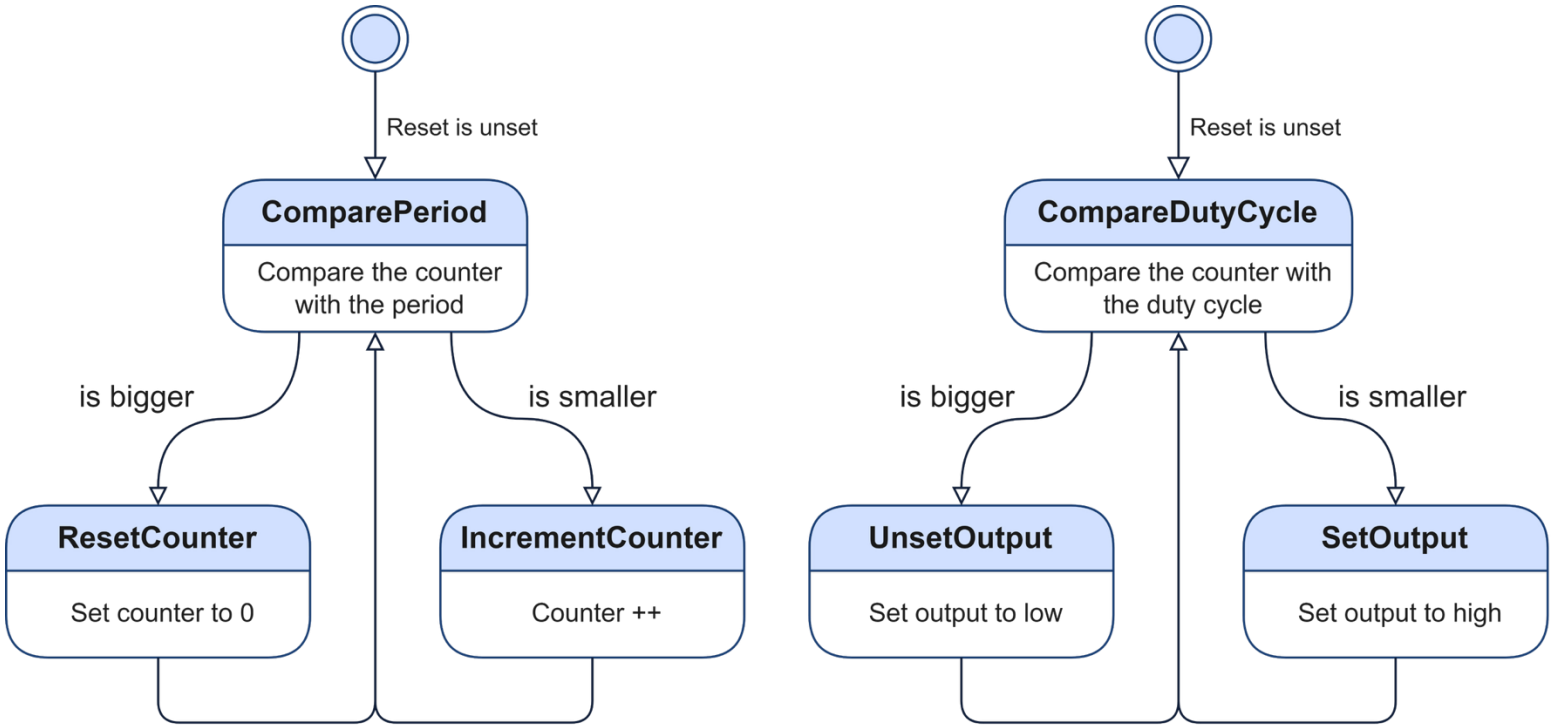
- **DShot FSM**
  - Encodes digital control frames (150/300/600/1200 kbps)
  - Built-in error detection, inter-frame gap handling
  - Deterministic timing → < 50 ns jitter



Multi-Protocol FSMs for ESC Control (Cont.)

Dedicated FSM IP Cores:

- **PWM FSM**
  - Free-running counter + compare logic
  - Generates precise duty cycles for analog-equivalent control
  - Hard-reset each cycle ensures consistency



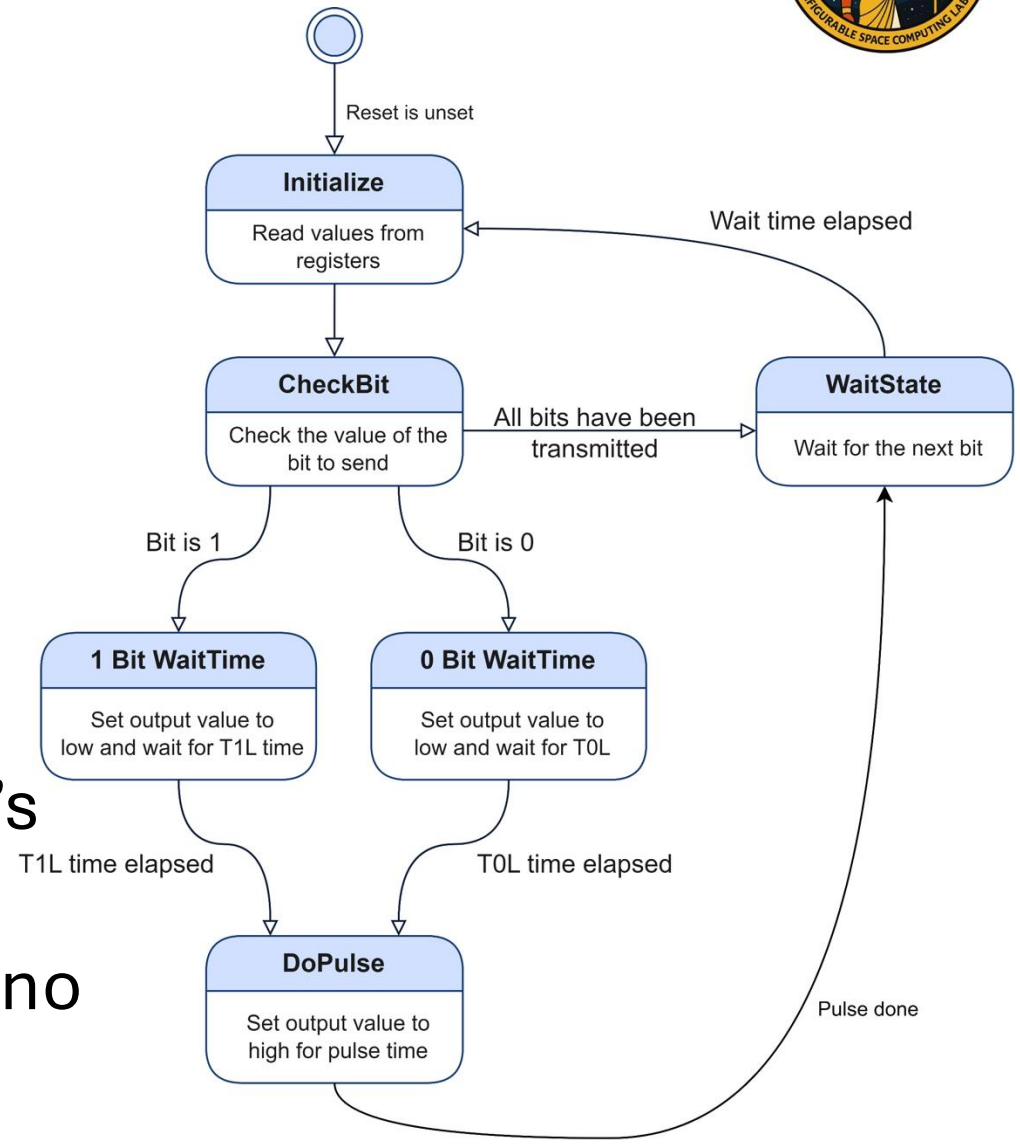
Multi-Protocol FSMs for ESC Control (Cont.)

Dedicated FSM IP Cores:

- **PPM FSM**
  - Serializes multiple channel pulses into one train
  - States: Initialize → DoPulse → WaitTime
  - Provides backwards compatibility with legacy ESCs

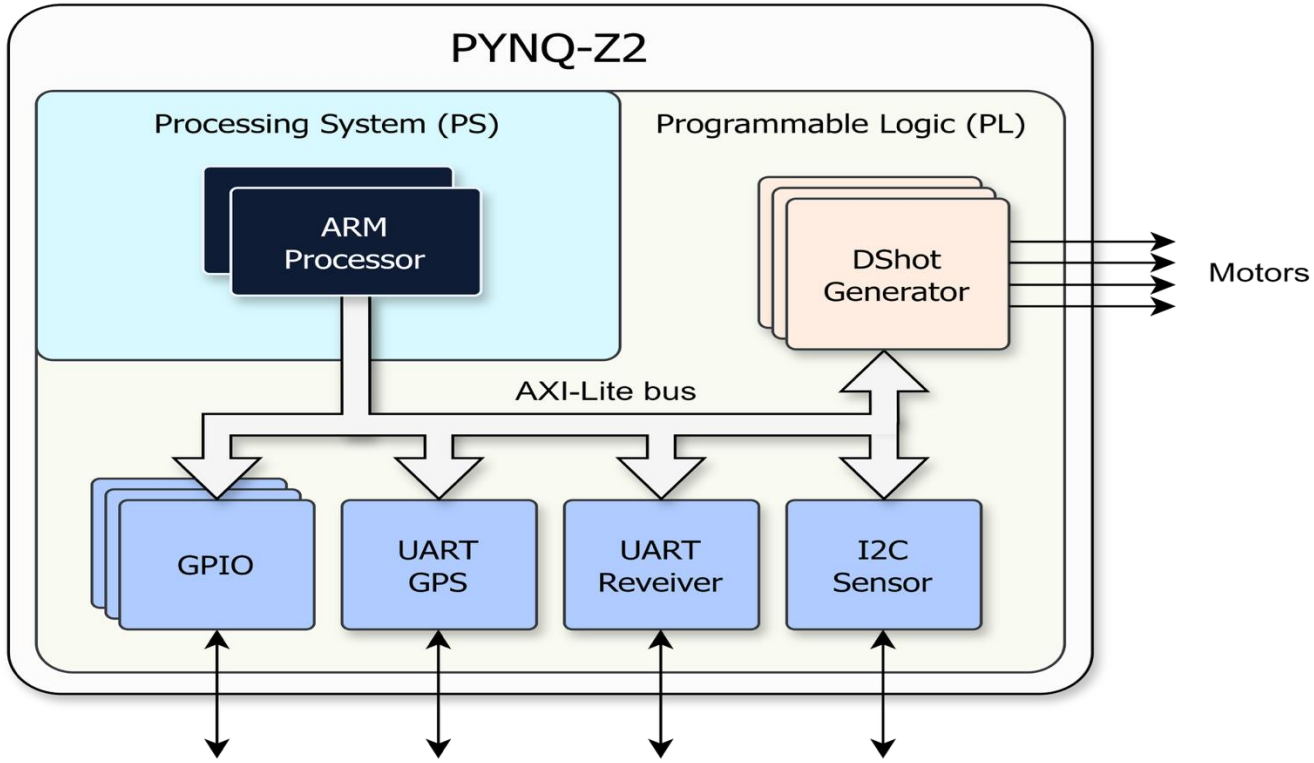
Hardware Protocol Selector:

- Crossbar switch in PL routes each channel's signal to the appropriate FSM
- Dynamic, per-channel protocol changing—no reprogramming required



Processing Unit: MicroBlaze vs. ARM Cortex-A9

Feature	MicroBlaze	ARM Cortex-A9
Max Channels	16	32
Control Execution	PID & ESC loops in FPGA soft-core	PID & ESC loops natively in PS
Telemetry & Profiling	Limited (PL-only)	Full AXI-Lite telemetry + AXI Timer profiling

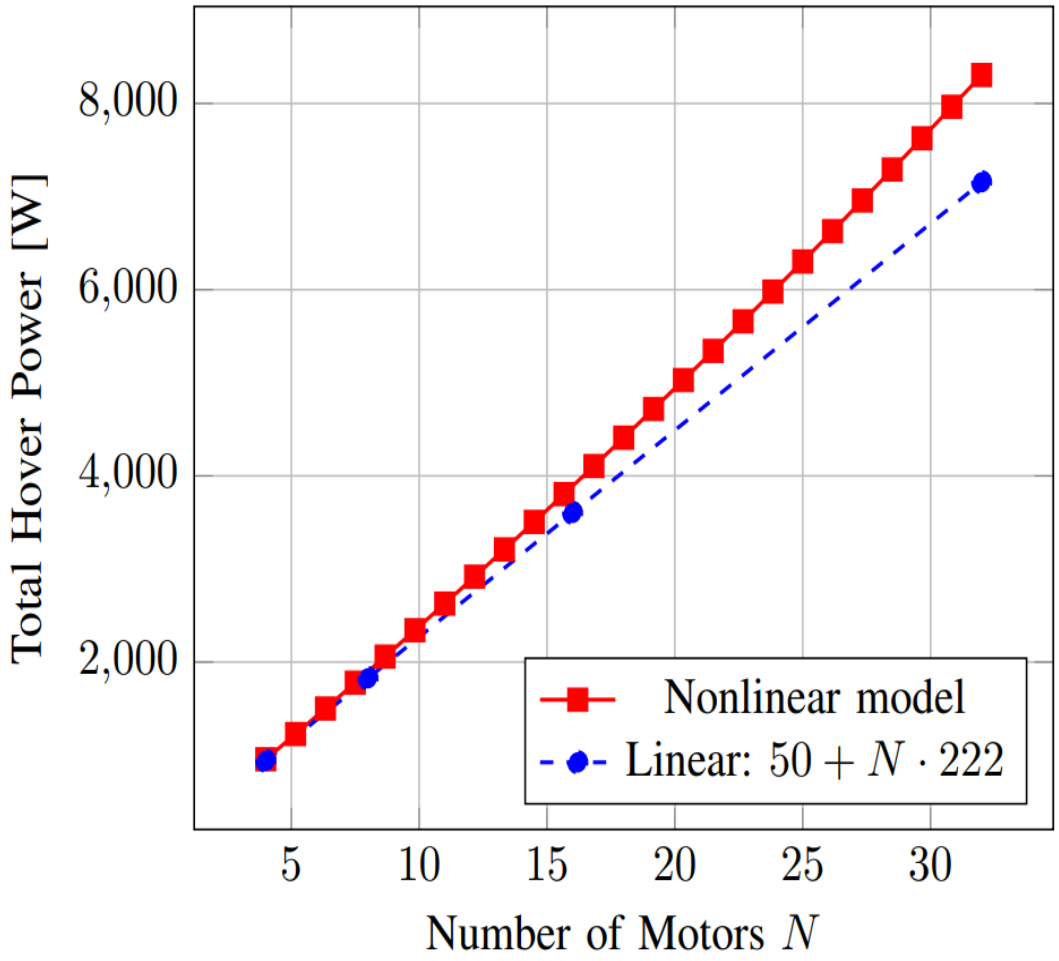


Power & Scalability

- **Hover-power model:**

$$P_{total}(N) = P_{static} + N \cdot P_h + R_{wir}(N \cdot Ihove)^2$$

- **Measured draw:**
  - **0.8** W/channel (MicroBlaze prototype)
  - 1.9 W/channel (ARM Cortex-A9 design
- **FPGA headroom:**
  - Only 11% LUTs used at 32 channels → room for TMR, scrubbing, extra logic



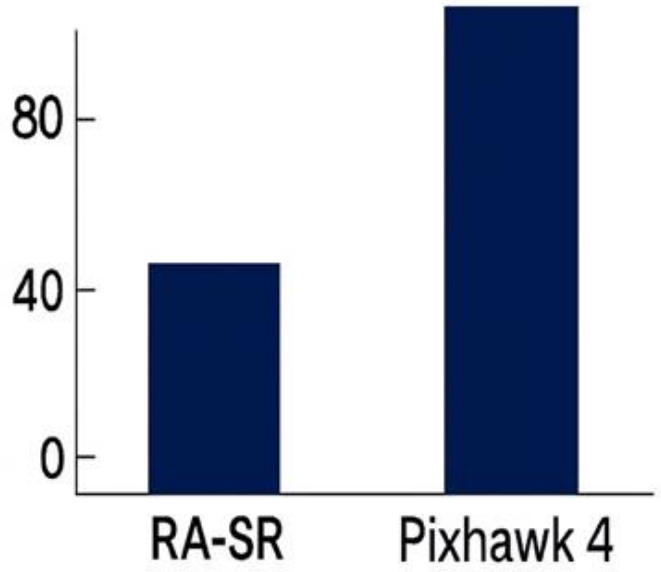
Hover-power scaling: nonlinear vs. linear model over $N = 4$–32.

Cost Analysis

Component	Cost(USD)
PYNQ-Z2 FPGA board(amortized)	3.13
Flycolor Francy2 50 A ESC	12.00
HUIOP 5010 750 KV motor	15.00
KingVal 12×4.5" propeller	3.00
Wiring, Connectors, fuses	5.00
Total per channel	38.18

Comparison

- ~$38/channel vs. ~$100/channel for a Pixhawk 4-based setup
- RA-SR delivers >2× more channels at ~⅓ the cost



Worst-case control-signal jitter comparison

System	Jitter
STM32F44 MCU (Pillai & Rao)	1.2 μs
Pixhawk 4 (STM32H743)	1 μs
Lee & Kim (MCU+FPGA)	0.5 μs
Wang & Chen (FPGA DShot)	<100 ns
Patel & Singh (FPGA PWM)	100 ns
RA-SR (this work)	**<50 ns**

Space Readiness

Key Validation & Qualification Steps:

- **EMI Testing**
  - Tesla-coil RF exposure → jitter increase < 5 ns
  - Verifies robustness against high-frequency interference

Thermal-Vacuum (TVAC)

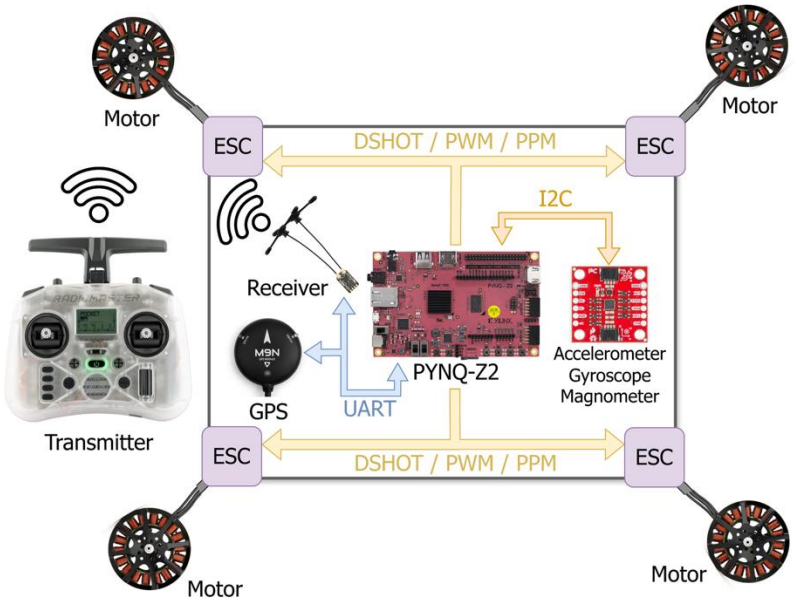
- −20°C to +60°C at 10^{-5} Torr
- Stable < 50 ns timing across full temperature range

Radiation Hardening Roadmap

- TMR & Scrubbing: Triple-modular redundancy in PL, periodic bitstream refresh
- Conformal Coating & MLI: Protect against outgassing, micrometeoroids
- Partial Bitstream Reconfiguration: On-orbit updates & fail-safe rollback

Flight Demonstration Plans

- High-altitude balloon proof-of-concept
- CubeSat-hosted electronics bay for in-orbit qualification



Conclusion & Impact

RA-SR highlights: <50 ns jitter, 16–32 ch, zero CPU, ≦ 1.9 W/ch, $38/ch

Performance: outperforms MCU, hybrid, and other FPGA designs

Future: Rad-hard FPGA port, TVAC, on-orbit reconfig, AI-driven control, flight demos

Acknowledgements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tapadh leat
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faafetai lava
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